

FIG. 1

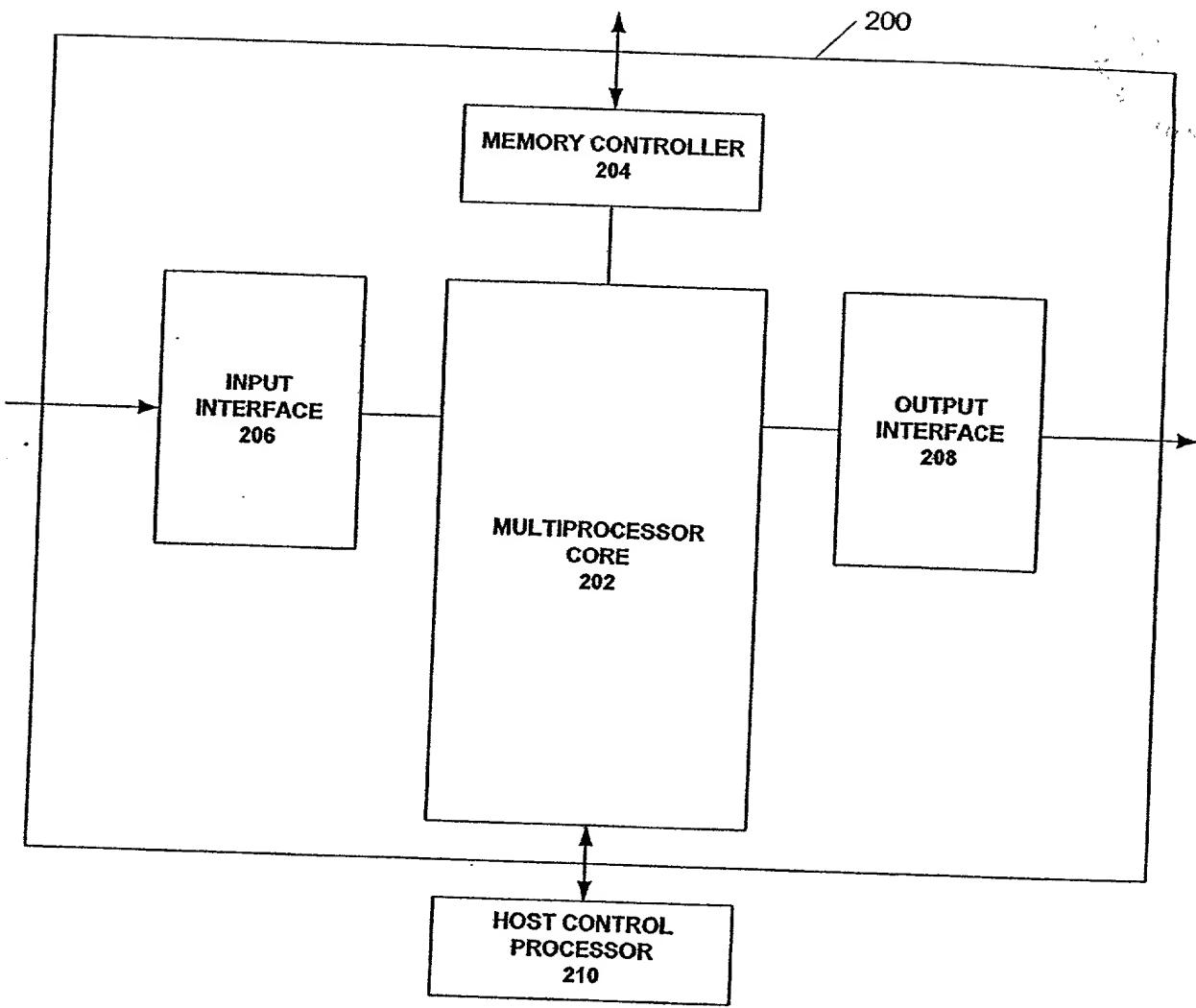


FIG. 2

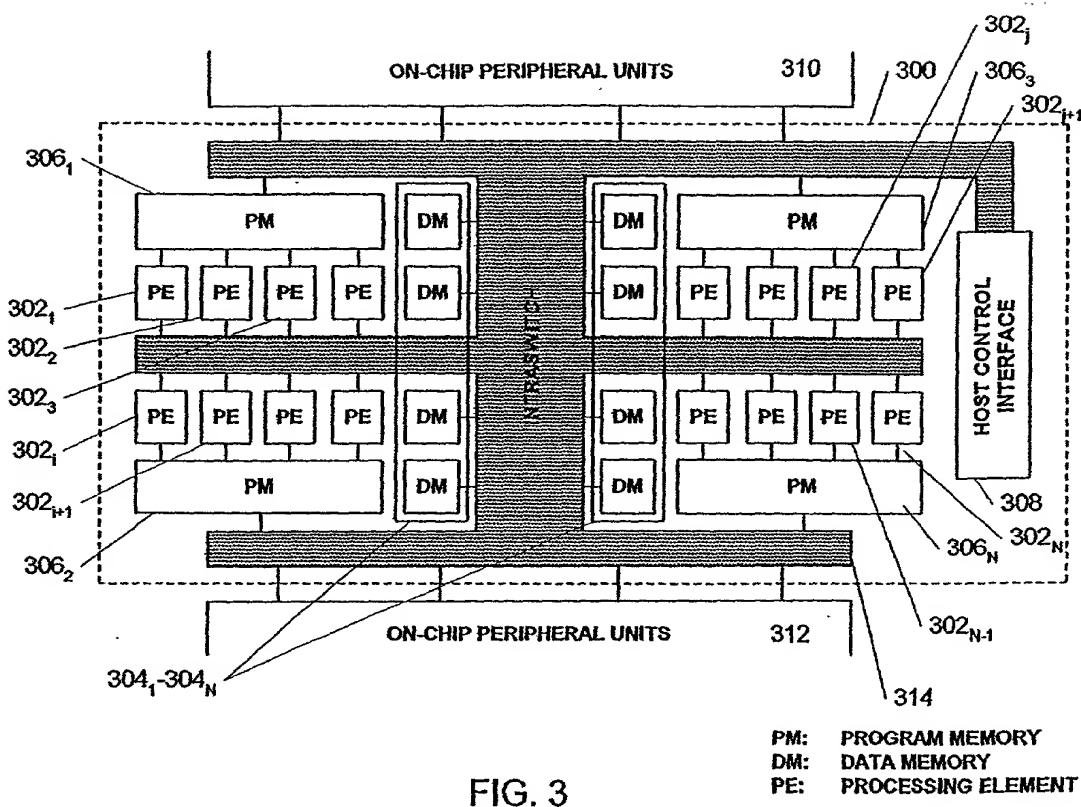


FIG. 3

PM: PROGRAM MEMORY
DM: DATA MEMORY
PE: PROCESSING ELEMENT

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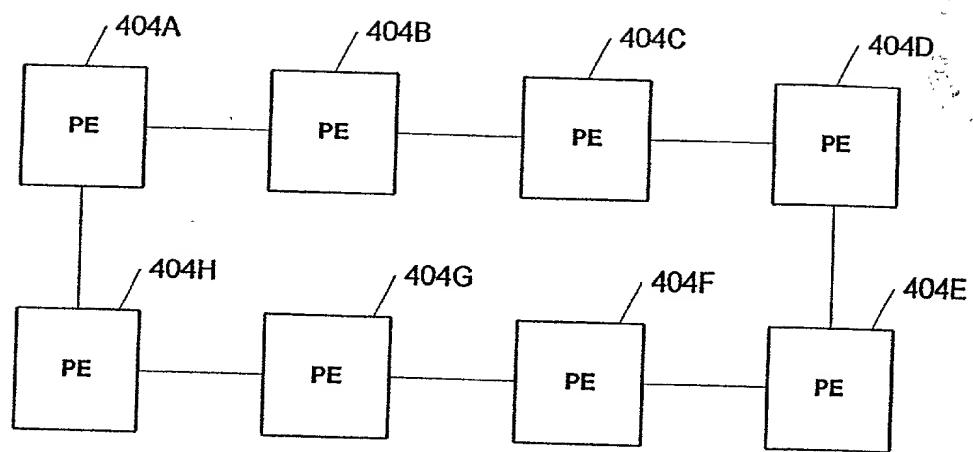


FIG. 4A

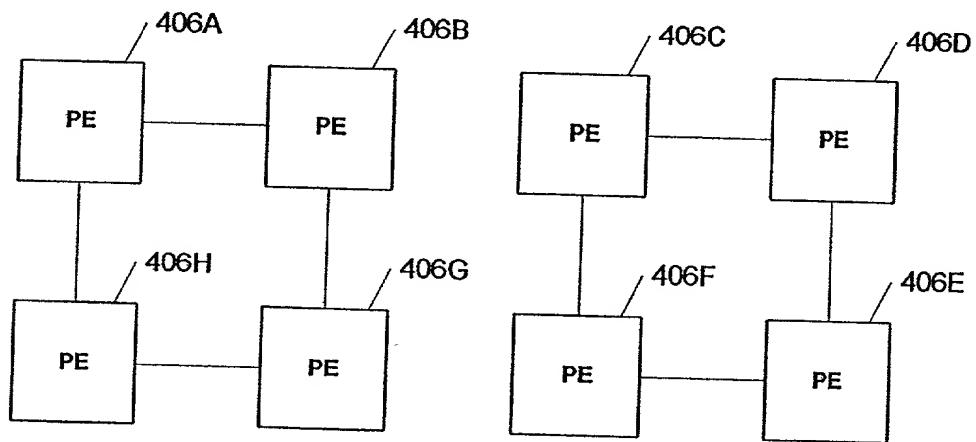


FIG. 4B

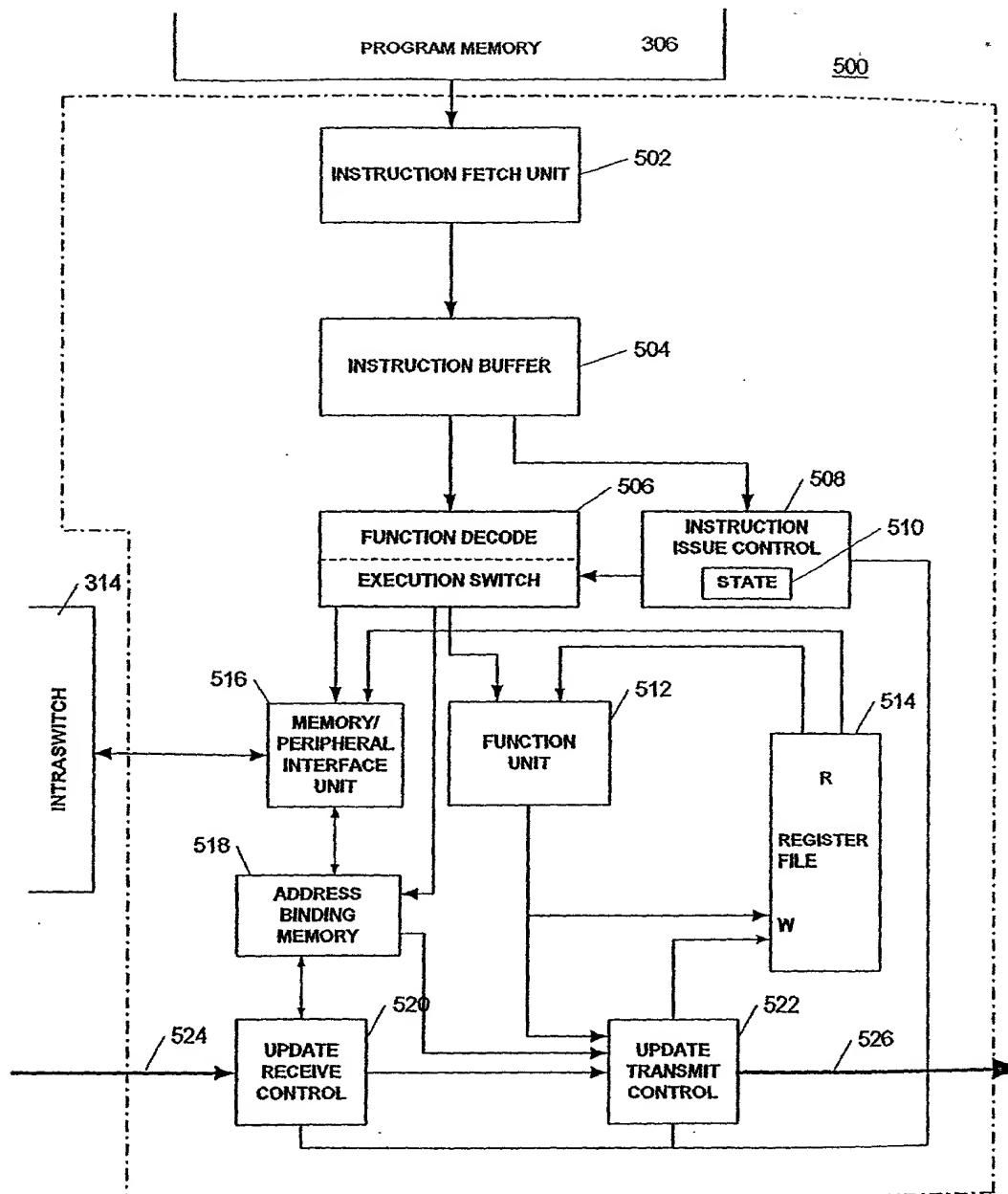


FIG. 5

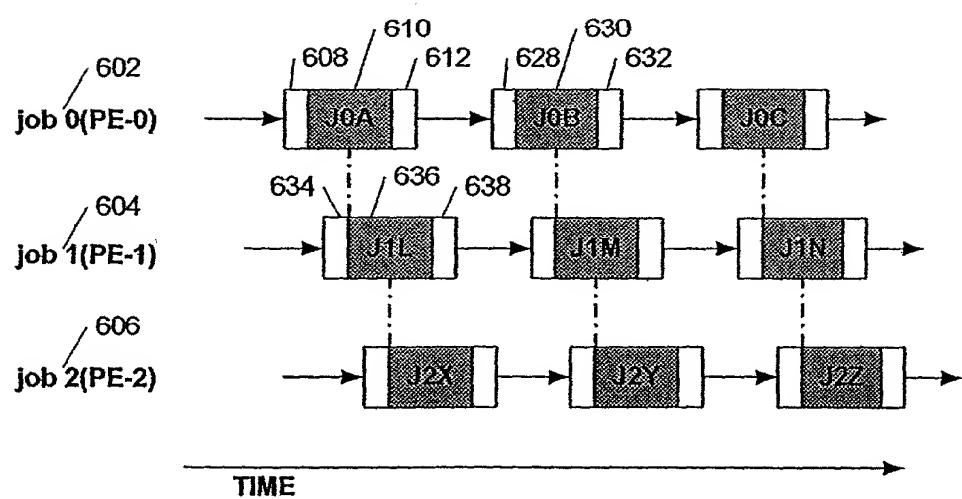


FIG. 6

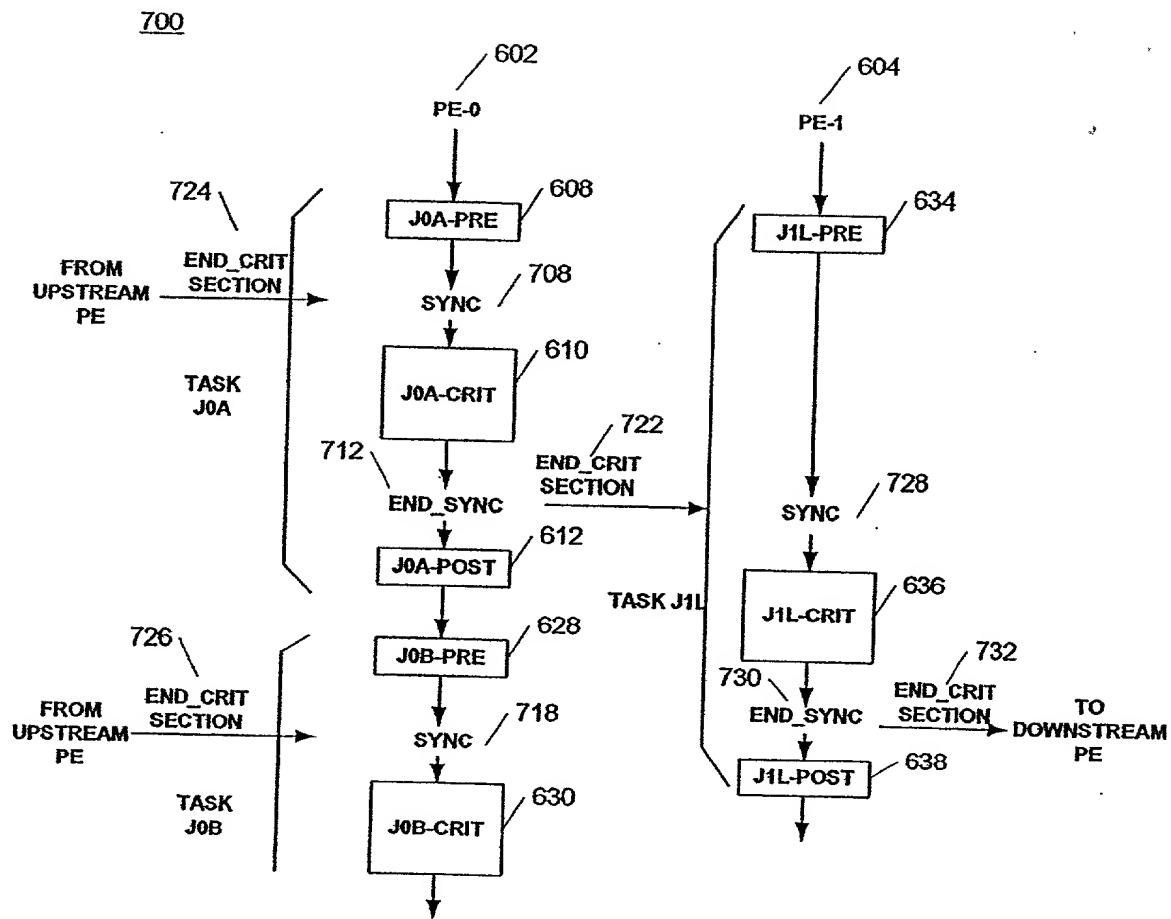


FIG. 7

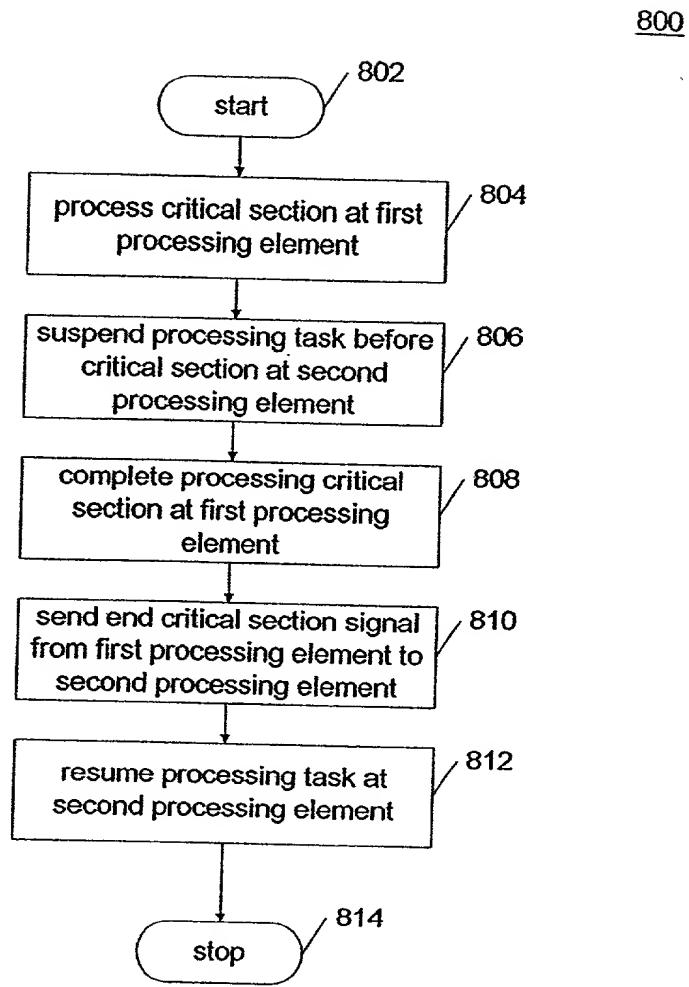


FIG. 8

900

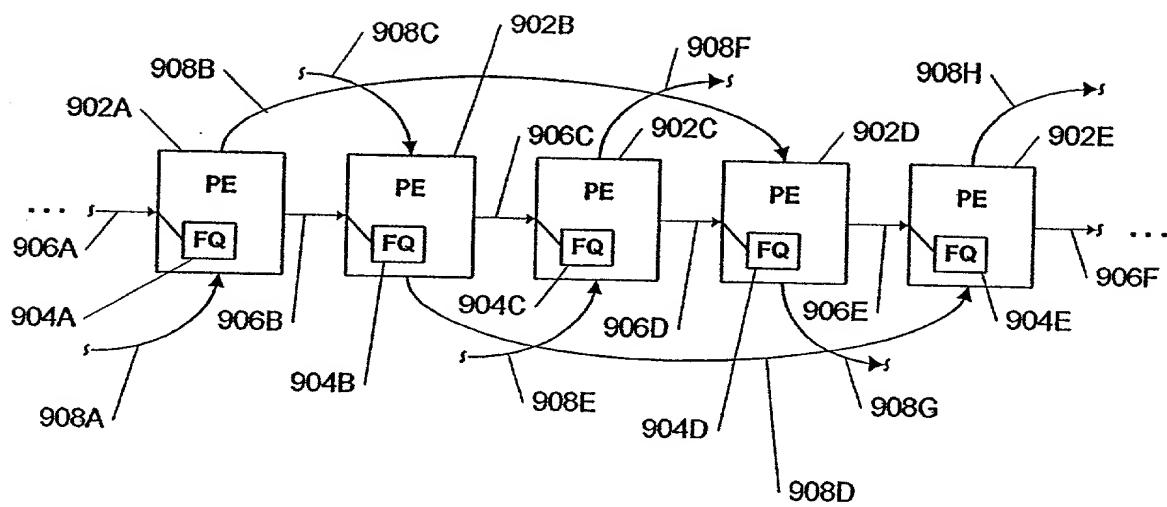
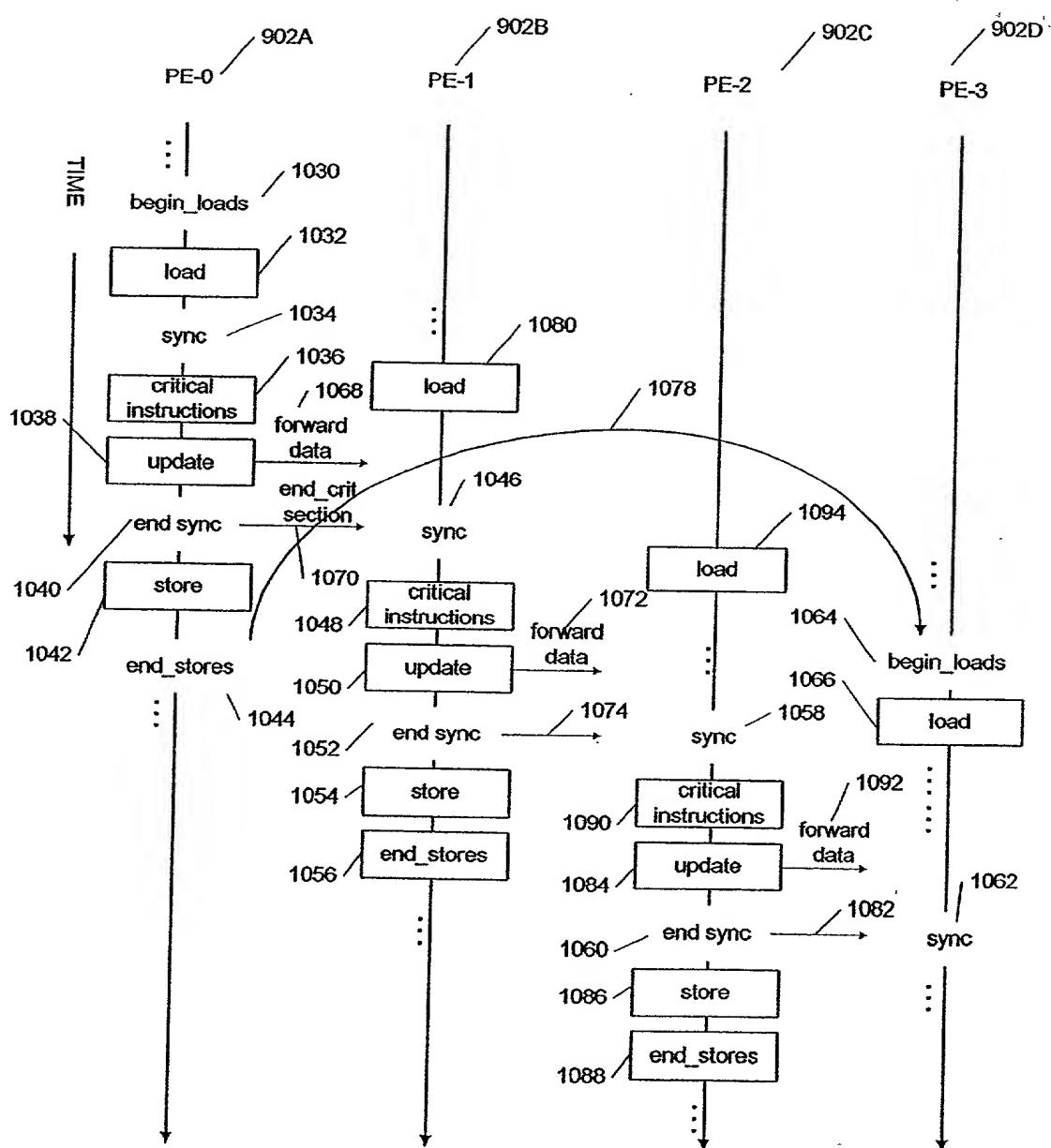


FIG. 9

FIG. 10

1000



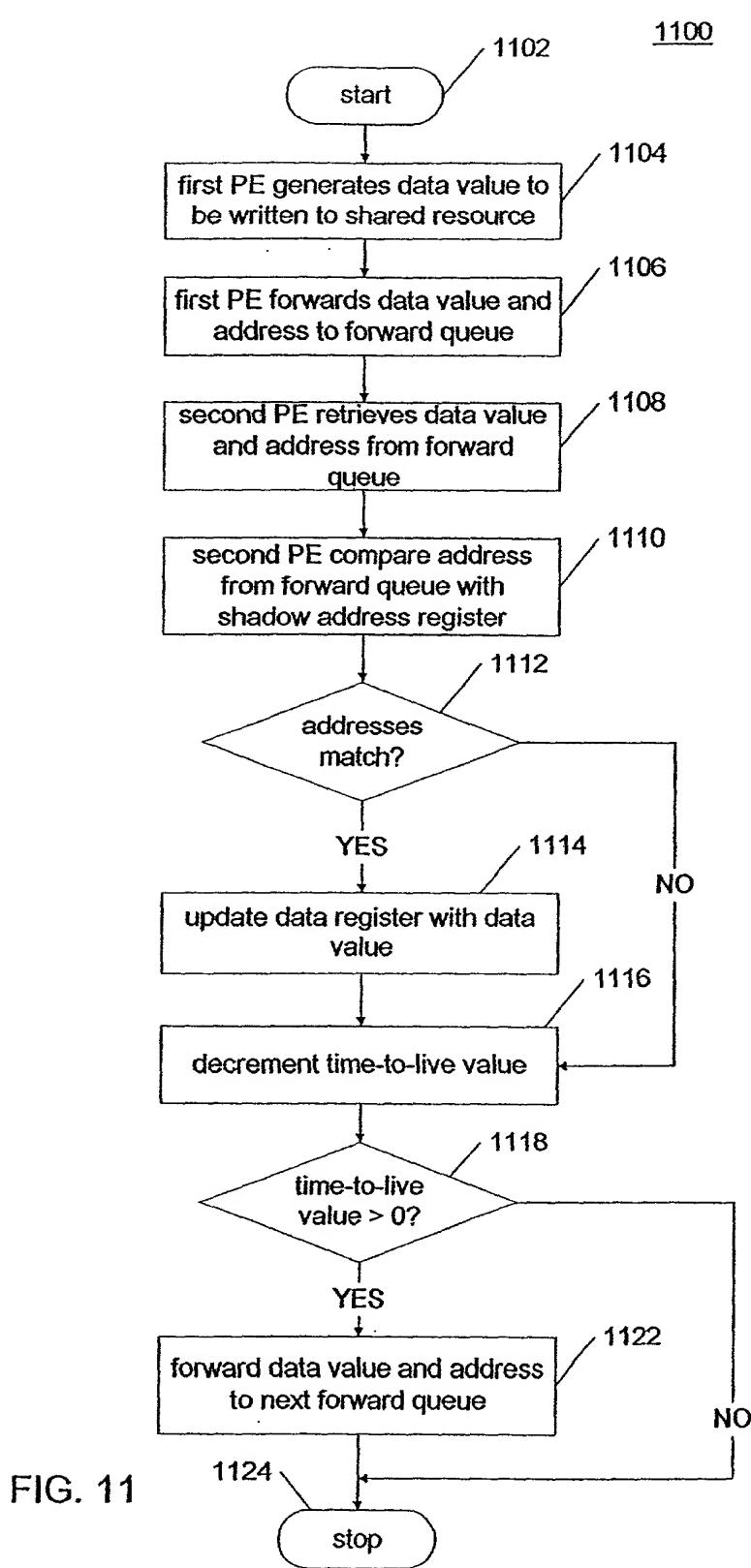


FIG. 11

1200

Diagram illustrating a memory table structure with 1200 as the header. The table has columns labeled DATA, ADDRESS, REGISTER #, TTL, and LAST UPDATE. The table contains four rows of data: D1 (ADDRESS A1, REGISTER # R1, TTL 3, LAST UPDATE F), D2 (ADDRESS A2, REGISTER # R2, TTL 2, LAST UPDATE F), D3 (ADDRESS A3, REGISTER # R3, TTL 4, LAST UPDATE F), and D4 (ADDRESS A4, REGISTER # R4, TTL 1, LAST UPDATE T). The table is enclosed in a border, and the entire structure is labeled 1200 at the top.

DATA	ADDRESS	REGISTER #	TTL	LAST UPDATE
D1	A1	R1	3	F
D2	A2	R2	2	F
D3	A3	R3	4	F
D4	A4	R4	1	T

FIG. 12

1300

Diagram illustrating a memory table structure with 1300 as the header. The table has columns labeled opcode, source 0, source 1, destination, update, sync, endstores, and beginloads. The table is enclosed in a border, and the entire structure is labeled 1300 at the top.

opcode	source 0	source 1	destination	update	sync	endstores	beginloads

FIG. 13

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